SOLE INVENTOR

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APPLICATION FOR
UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, Sung Gyu PYO, a citizen of the Republic of Korea, residing at Hyundai Apt. 102-1203, Changjeon-Dong, Ichon-Shi, Kyungki-Do, Republic of Korea, have invented a new and useful METHOD OF FORMING A METAL WIRING IN A SEMICONDUCTOR DEVICE, of which the following is a specificati n.

METHOD OF FORMING A METAL WIRING IN A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Technical Field

A method of forming a metal wiring in a semiconductor device is disclosed. More particularly, the disclosure relates to a method of forming a metal wiring in a semiconductor device by which copper can be selectively filled and an increase of the via resistance in the copper wiring can be prevented with a diffusion prevention film. Still more specifically, a chemical enhancer layer is formed and a damascene pattern of an ultra-fine structure is then filled with copper using a copper precursor.

Description of the Prior Art

As the integration level of semiconductor devices is increased and its signal transfer speed is lowered, there has been an effort to use copper as a metal wiring for transferring current because copper has a substantially lower resistivity than conventional aluminum and, conversely, copper has good electrical conductivity.

However, copper has a disadvantage that the diffusion speed of copper into a silicon oxide used as an insulating film in a semiconductor device is faster than aluminum. Copper atoms that diffuse into the silicon oxide degrades transistors and capacitors in the semiconductor device and thus increase the leakage current. As a result, a diffusion prevention film for preventing diffusion of copper is required. In a dual damascene structure, however, when a copper wiring is formed, as the diffusion prevention film exists in the bottom of the via contact, it functions to increase the via resistance in the copper wiring. Therefore, if a prevention barrier metal having a low resistivity is not suitably selected, it is thought that the effect of resistance will be great and dishing and erosion may be caused by the difference of a selective ratio with the diffusion barrier film during CMP process.

In addition, due to the rapid higher performance and miniaturization of next-generation semiconductor devices, there is a trend toward forming a copper wiring using CVD. However, filling of copper using the CVD method has problems that the deposition speed is slow and the cost is high.

Recently, there is a growing interest in filling of copper wiring using chemically enhanced chemical vapor deposition (CECVD) method. This method, however, has a problem in that the chemical enhancer must be uniformly sprayed and a selective filling method must be applied by which the chemical enhancer is distributed at a specific location, which is difficult to employ.

SUMMARY OF THE DISCLOSURE

A metal wiring in a semiconductor device is disclosed that is capable of preventing an increase in the via resistance by forming a diffusion prevention film on the sidewall of a damascene pattern in the form of a spacer. The method also facilitates select partial filling of the damascene pattern using a copper precursor by selectively forming a chemical enhancer layer within the damascene pattern using a selective reaction property of the chemical enhancer.

The disclosed method of forming a metal wiring in a semiconductor device is characterized in that it comprises: providing a substrate in which an interlayer insulating film consisted of first, second and third insulating films are formed on a lower metal layer; forming a damascene pattern consisting of a trench and a via on the interlayer insulating film; forming a diffusion prevention film spacer on the sidewall of the trench and the via; selectively forming a chemical enhancer layer on the second insulating film constituting the bottom of the trench and on the lower metal layer constituting the bottom of the via; forming a copper layer by means of chemical vapor deposition method; and performing a hydrogen reduction annealing and a chemical mechanical polishing process to form a copper metal wiring.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

Figs. 1A through 1C are cross-sectional views sequentially illustrating a method of forming a metal wiring in a semiconductor device.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

The disclosed method will be described in detail by way of a preferred embodiment with reference to accompanying drawings.

Referring now to Figs. 1A through 1C, a method of forming a metal wiring in a semiconductor device will be below explained in detail.

Referring now to Fig. 1A, a first interlayer insulating film 20, a lower metal layer 30 and a second interlayer insulating film 40 are sequentially formed on a semiconductor substrate 10 in which various components for forming a semiconductor device are also formed. The second interlayer insulating film 40 consists of a first insulating film 40a, a second insulating film 40b and a third insulating film 40c. Of them, the second insulating film 40b comprises a nitride material and serves as an etch prevention film for preventing the first insulating film 40a from being etched upon formation of a trench that is formed during the process of forming a damascene pattern in the second interlayer insulating film 40. Then, a damascene pattern consisting of a trench and a via is formed in the second interlayer insulating film 40 and a cleaning process is then performed to remove an oxide layer left on the surface of the lower metal layer 30 that is exposed by the damascene pattern. Next, a diffusion prevention film is formed having a thickness ranging from about 50 to about 500 Å on the second interlayer insulating film 40 including the exposed lower metal layer 30. The diffusion prevention film is blanket etch processed so that the diffusion prevention film can be remained only at the sidewall of the damascene pattern, thus forming a diffusion prevention film spacer 50.

The first and third insulating films 40a and 40c are formed of oxide materials having a low dielectric constant and the second insulating film 40b is formed from a nitride material. The trench and via formed in the second interlayer insulating film 40 are formed in a double damascene pattern. The cleaning process may employ RF plasma in case that the lower metal layer 30 is made of W, Al, etc. or employ a reactive cleaning method in case that the lower metal layer 30 is made of Cu. The diffusion prevention film may be formed using at least one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN, CVD WN, CVD TiAlN, CVD TiSiN and CVD TaSiN. The reason by which the diffusion prevention film is formed in the shape of a spacer is that the via resistance is increased

by the resistance component of the diffusion prevention film if the diffusion prevention film is formed including the surface of the lower metal layer 30.

In other words, the diffusion prevention film spacer 50 not only sufficiently plays its role to prevent outward diffusion of copper atoms since it covers the first and third insulating films 40a and 40c within the damascene pattern but also can lower the via resistance since the surface of the lower metal layer 30 is exposed. The diffusion prevention film spacer 50 may be formed of a nonconductor such as a silicon nitride (SiN) film or a silicon oxynitride (SiON) film since it does not exist in the bottom of the via.

Referring now to Fig. 1B, a chemical enhancer layer 60 is formed on the entire structure including the lower metal layer 30. The chemical enhancer layer 60 has a selective reaction property in which it rarely reacts with an oxide material and well reacts with a nitride material and a metal. Therefore, the chemical enhancer layer 60 is not formed on the third insulating film 40c made of an oxide material and is formed only on the second insulating film 40b made of a nitride material and the lower metal layer 30, as shown.

Sub A1 The chemical enhancer layer 60 is formed in thickness ranging from about 50 to about 500 Å. Catalysts for forming the chemical enhancer 60 may include one of I (iodine)-containing liquid compounds such as CH_3I, C_2H_5I, CD_3I, CH_2I_2 etc., Hhfac1/2H_2O, Hhfac, TMVS, pure I_2, I (iodine)-containing gas and water vapor, and is performed at the temperature ranging from about -20 to about 300°C for a time period ranging from about 1 to about 600 seconds. Also, the catalysts may include F, Cl, Br, I, At of a liquid state and F, Cl, Br, I, At of a gas state, which are Group VII elements in the Periodic Table.

Referring now to Fig. 1C, a copper layer is formed on the second interlayer insulating film 40 including the damascene pattern by means of metal organic chemical vapor deposition (MOCVD) method using at least one of all the precursors of hfac series such as (hfac)CuVTMOS series, (hfac)CuDMB series, (hfac)CuTMVS series, etc., so that the damascene pattern is filled with copper. As the chemical enhancer layer 60 is formed on the second insulating film 40b and the lower metal layer 30, the speed by which copper is deposited into the damascene pattern is much faster than the speed by which copper is deposited on the third insulating film 40c. Thus, a selective copper deposition into the damascene pattern can be made. The

above selective deposition process may be performed in all the deposition equipments having a vaporizer of direct liquid injection (DLI), control evaporation mixer (CEM), orifice scheme and spray scheme. Thereafter, a hydrogen reduction annealing process is performed and the copper layer deposited on the third insulating film 40c is then removed by chemical mechanical polishing (CMP), thus forming a copper wiring 70. Though, the copper layer may be formed on the third insulating film 40c, it is accelerated by the chemical enhancer layer 60. Thus, as the copper layer deposited on the third insulating film 40c is very thin, it can be easily removed by CMP process.

In the above embodiment, it was explained that copper (Cu) is used as a material for forming a metal wiring. However, it should be noted that other metals such as aluminum or tungsten may be used instead.

As mentioned above, the present invention forms a diffusion prevention film in the form of a spacer, forms a chemical enhancer layer selectively within a damascene pattern and then deposits copper to form a wiring. Therefore, the present invention has outstanding effects that it can reduce the via resistance component and thus improve the operating speed and reliability of devices.

The present invention has been described with reference to a particular embodiment in connection with a particular application. Those having ordinary skill in the art and access to the teachings of the present invention will recognize additional modifications and applications within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications, and embodiments within the scope of the present invention.